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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,566	03/29/2004	Jerome J. Cartmell	EMS-07501	1387

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EXAMINER	
VERBRUGGE, KEVIN	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,566	CARTMELL ET AL.	
	Examiner	Art Unit	
	Kevin Verbrugge	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-15 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10,12-15 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This final Office action is in response to the amendment received 9/14/06 which canceled claims 2, 11, and 16. Claims 1, 3-10, 12-15, and 17-20 are pending. Applicants' arguments have been considered but are not persuasive, therefore the art rejection is repeated and made final. All rejections and objections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 10, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,761,705 to DeKoning et al.

DeKoning shows the claimed data storage device as RAID storage subsystem 100 in Fig. 1.

He shows the claimed plurality of disk drives as disk drives 110.

He shows the claimed internal volatile memory as cache memory 116.1 and 116.2 and teaches in several places that the cache memories include volatile and non-

volatile portions (see column 8, lines 5-22, column 9, lines 53-58, and column 11, lines 23-26 and lines 49-51).

Finally, he shows the claimed directors as redundant disk array controllers (RDACs) 118.1 and 118.2. The RDACs perform the claimed operations as taught throughout the specification and summarized at column 2, line 30 through column 3, line 58.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-9, 12-14, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,761,705 to DeKoning et al.

DeKoning does not explicitly teach locking or testing the memory, however, these are standard memory operations and it would have been obvious to one of ordinary skill in the art at the time the invention was made to include them in DeKoning's device. Locking a portion of memory to prevent additional access to that portion of memory ensures that no changes will be made to memory to interfere with the current write that is being performed, thereby ensuring data accuracy. Testing a memory before using it

reduces the chance of failures during use since a memory that fails testing can be flagged and replaced before being put into use.

Response to Arguments

Applicants essentially have only one argument, namely that DeKoning does not teach or suggest the newly added limitations of claims 1, 10, and 15 (see page 14, first full paragraph). The new limitations are essentially former claims 2, 11, and 16, so essentially what Applicants are arguing is that DeKoning does not teach or suggest original claims 2, 11, and 16.

As background, a few relevant passages of DeKoning will be quoted here (emphasis added) so that the clear teachings of DeKoning can be discussed in detail below:

> The methods of the present invention then coordinates [sic] the "late check-in" of the second controller by assuring consistency of the redundant caches during processing of host computer I/O request by the first controller. (column 2, lines 45-49)
>
> If one of the control modules indicates a foreign status or indicates an invalid cache due to a "bad" battery subsystem, then the first control module continues to perform host computer I/O requests in a "write-through" mode until the two cache memory modules are again restored to synchronization. The caches are synchronized by appropriate copy operations in the background as host computer I/O requests are processed by the first controller in the write-through mode. (column 3, lines 17-25)
>
> After the brief timeout, the first controller will switch to a "write-through" mode of operation as it awaits the "late check-in" of the second controller. This feature of the present invention enables the RAID subsystem to process host computer I/O requests (though in a degraded mode of operation) while the redundant pair of control modules synchronize their respective caches. (column 3, lines 33-40)

> It is a further object of the present invention to provide methods and associated apparatus for synchronizing redundant pairs of cached control modules while a first control module of each pair continues to process host computer I/O requests. (column 3, lines 51-55)
>
> The present invention comprises methods, expressed as state machines operable within each of the pair of RDACs, which assure synchronization of the redundant cache memories while reducing the initialization time during which the RAID subsystem is unavailable for processing of host computer system I/O requests. (column 6, lines 62-67)
>
> In the write-through cache mode all write I/O requests are immediately posted to the disk array 108 of the RAID subsystem. (column 9, lines 32-34)
>
> Once the coherency flag is cleared, processing continues with elements 434 and 436 to process I/O requests in the write-through mode while awaiting late check in of the alternate RDAC 118.2. In particular, element 434 processes any outstanding write requests and posts them directly to the disk array writing through the cache 116.1. (column 10, lines 25-30)
>
> If element 606 determines that the cache 116.2 of the second RDAC 118.2 is usable or if element 610 determines that the copy of the cache from the alternate (first) RDAC 118.1 was successful (thereby synchronizing the redundant caches), then processing continues with element 616 to complete processing to synchronize the duplicate, redundant caches. In particular, element 616 is operable to recovery [sic] all volatile cache management data structures (e.g., CCBs) from the non-volatile portion of the cache 116.2 now synchronized with the alternate (first) cache 116.1. Processing then continue [sic] with element 614, as above, to commence processing of I/O requests in the write-back mirrored cache mode. (column 11, lines 43-56)

From this last passage and the rest of DeKoning's disclosure, it is clear that DeKoning's device normally operates in a write-back mirrored cache mode, which is to say that data written to cache 116.1 is mirrored in cache 116.2 immediately and this data is written in disk array 108 later (written back to disk). This is in contrast to the degraded mode of operation when there has been a failure of cache 116.2, for example, and cache 116.1 switches to write-through mode.

Contrary to what Applicants seem to be arguing at the top of page 14, write-through mode is not where write requests are posted to the disk array "rather than to the memory caches" but rather write-through mode is where write requests are posted to the disk array and at least one cache at the same time. This is the normal meaning of write-through mode in the art and although the column 9 passage cited above only mentions that data is posted to the disk array, DeKoning clearly teaches in the column 10 passage cited above that the data is written to the disk array and cache 116.1.

Therefore, in what DeKoning calls the degraded mode, data is written through (and into) cache 116.1 and into disk array 108 until cache 116.2 gets repaired or replaced and is suitable for data storage. At that time, "the first control module continues to perform host computer I/O requests in a 'write-through' mode until the two cache memory modules are again restored to synchronization. The caches are synchronized by appropriate copy operations in the background as host computer I/O requests are processed by the first controller in the write-through mode" (column 3, lines 17-25).

In other words, once cache 116.2 is available again, data from cache 116.1 are copied to cache 116.2 in background copy operations. During these background copy operations, cache 116.1 responds to the host computer I/O requests in a write-through mode so that any writes are immediately stored in the cache and the disk array, providing security against data loss from the volatile cache 116.1, should it fail. Reads are provided from cache 116.1 as they normally are.

Once cache 116.1 completes the copying of its data to cache 116.2, normal write-back mirroring mode operation can resume since data protection is provided by the caches containing identical copies of the data. If one cache fails, the other cache still has the data.

Specifically regarding the claim language (of claim 1, for simplicity, but relevant to claims 10 and 15 as well), cache 116.1 is the non-faulting memory of the claims while cache 116.2 is the faulting memory.

Initially, cache 116.1 services all host computer I/O requests as claimed since cache 116.2 has faulted.

DeKoning's device determines that cache 116.2 hardware has been replaced as claimed.

Once this occurs, DeKoning's device causes data to be copied from cache 116.1 to cache 116.2 while data is being read from and written to cache 116.1 as claimed (that is why DeKoning calls these copy operations "background" copy operations).

In response to a write being performed to cache 116.1 while data is being copied to cache 116.2, this write is performed to cache 116.1 and to cache 116.2 as claimed. It is not clear from DeKoning's disclosure whether this write is performed to cache 116.2 immediately or later as part of the background copy operations, but both alternatives meet the broad language of the claims. In other words, even if DeKoning's device does not perform this write to cache 116.2 until later as part of the background copy

operations, his device is still "causing the write to be performed to the non-faulting memory and the new memory" as claimed.

Finally, once the background copy operations are completed, the system is put in the write-back mirroring mode and all new writes are performed to both caches as claimed.

Conclusion

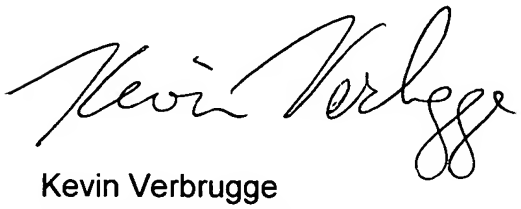
The method claims are grouped and rejected with the apparatus claims because the steps of the method are met by the disclosure of the apparatus and methods of the reference(s) as discussed above.

Any inquiry concerning this Office action should be directed to the Examiner by phone at (571) 272-4214.

Any response to this Office action should be labeled appropriately (including serial number, Art Unit 2189, and type of response) and mailed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, hand-carried or delivered to the Customer Service Window at the Randolph Building, 401 Dulany Street, Alexandria, VA 22313, or faxed to (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.



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Art Unit 2189